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Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

U.S. UTILITY Patent Application

<p><i>ML</i></p> <p>O.I.P.E.</p> <p>SCANNED <i>AC3</i> Q.A. <i>AA</i></p>	PATENT DATE
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APPLICATION NO. 09/916598	CONT/PRIOR	CLASS 265 710	SUBCLASS 03	ART UNIT 2818 281	EXAMINER Auer
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APPLICANTS

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TITLE

Cache coherent split transaction memory bus architecture and protocol for a multi processor chip device

ISSUING CLASSIFICATION												
ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED		
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		NOTICE OF ALLOWANCE MAILED		
	<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____		ISSUE FEE <table border="1"> <tr> <td>Amount Due</td> <td>Date Paid</td> </tr> </table>		Amount Due
Amount Due	Date Paid				
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)		ISSUE BATCH NUMBER		
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